In the claims:

Please amend the claims as follows:

1-3. (Canceled)

4. (New) A multiple-clock-domain microprocessor comprising:

a plurality of domains;

for each of the plurality of domains, a clock for separately generating a clock signal at a frequency for that domain, the frequency being dynamically changeable independently of the frequencies of the clock signals generated for others of the plurality of domains; and

for each of the plurality of domains, a voltage input for receiving a voltage which is dynamically changeable independently of the voltages applied to said others of the plurality of domains.

5. (New) The microprocessor of claim 4, wherein each said clock comprises a phase-locked loop, and wherein the microprocessor further comprises means for receiving an externally generated clock signal and for supplying the externally generated clock signal to each said phase-locked loop.

6. (New) The microprocessor of claim 4, wherein there are at least four of said domains.

7. (New) The microprocessor of claim 4, wherein the microprocessor is programmed to determine a slack in processing in one of the domains and to reduce the clock frequency and the voltage in said one of the domains to reduce the slack.

8. (New) The microprocessor of claim 4, further comprising a queue for communication between at least two of the domains.

9. (New) The microprocessor of claim 8, wherein the queue has a *Full* flag and an *Empty* flag, and wherein the microprocessor is programmed to prevent a write to the queue when

the *Full* flag is asserted, until the *Full* flag is deasserted; and to prevent a read from the queue when the *Empty* flag is asserted, until the *Empty* flag is deasserted.

10. (New) The microprocessor of claim 9, wherein the queue is implemented as a dual-ported SRAM.

11. (New) A method of operating a microprocessor, the method comprising:

(a) providing a plurality of domains in the microprocessor;

(b) clocking each of the domains separately at a clock frequency;

(c) applying a voltage to each of the domains separately;

(d) operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another; and

(e) dynamically controlling the clock frequency and the voltage in each of the plurality of domains independently of the clock frequencies and the voltages in others of the plurality of domains.

12. (New) The method of claim 11, wherein step (e) comprises:

(i) determining a slack in processing in one of the domains; and

(ii) reducing the clock frequency and the voltage in said one of the domains to reduce the slack.

13. (New) The method of claim 11, wherein step (d) comprises providing a queue for communication between at least two of the domains.

14. (New) The method of claim 13, wherein the queue has a *Full* flag and an *Empty* flag, and wherein step (d) further comprises:

preventing a write to the queue when the *Full* flag is asserted, until the *Full* flag is deasserted; and

preventing a read from the queue when the *Empty* flag is asserted, until the *Empty* flag is deasserted.

15. (New) The method of claim 11, wherein there are at least four of said domains.